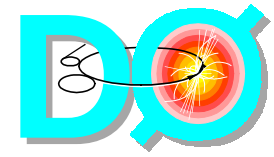

L1Muo Status and Plans

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Some D0 Meeting
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L1MU In a Nutshell

- All L1MU and nearly all MCEN hardware installed
- No L1MU readout problems at high rates (500 Hz)
- L1MU and MCEN Algorithms
  - Increased CF scintillator-only efficiency by ~25%
  - Implemented several low P_T dimuon triggers
  - Studying loose and tight PDT and MDT triggers with data
  - Measured rates for the above
- Current L1MU Strategy
  - Optimize scintillator-only and wire-only triggers with data
  - De-emphasize L1CFT.L1MUO until the fall

MCEN Status

- Hardware
  - All MCON's installed (since 10/01)
  - 42/48 MCEN's installed
- Hardware Problems
  - SRQ timeout errors in N B/C crate
  - Event building integrity
    - Crate loading problem?
    - Slow progress due to few accesses
- MDT Centroid Algorithms
  - Installed and used to form loose (A) and tight (AB) MDT triggers
  - Monitored in data with tsim

MCEN Plans

- **Priorities**
  - Understand and fix readout problems
  - Repair and certify remaining MCEN's
    - same engineer for both
  - Re-do MDT centroid equations with correct muon geometry
  - Move monitoring to online
  - "Everything else"

L1MU Status

- Hardware
  - Complete
- Hardware problems
  - No serious ones however we are still checking readout integrity
  - TF is *still* not at spec L1 decision latency
- L1MU algorithms
  - Final FPGA framework logic installed
    - Makes future changes to algorithms very simple
  - Loose and tight scintillator-only and wire-only algorithms in place
  - Optimizing these using data

L1MU High Pt Algorithms

- Single muon, loose and tight, scintillator-only (05) and/or wire-only (10) triggers in place
- Increased CF05 trigger efficiency by ~25%
  - Bottom octant improvements not yet downloaded
- Increase in EF05 trigger efficiency via AB or BC triggers aborted due to high rates
  - Data analysis in progress
- CF10 and EF10 triggers are in place and being "tagged" in the trigger
  - Data analysis in progress

L1MU Low Pt Algorithms

- Dimuon, loose and tight, scintillator-only (05) triggers in place
  - Also 2 loose muons plus 1 tight muon
- Dimuon, loose and tight, wire-only (10) triggers not optimized
  - Will eventually use centroid-confirmed scintillator hits
  - Studies for “count-to-two” with wire centroids in progress
- Manpower request to B group
  - Data and MC “count-to-two” trigger studies
  - Not for beginners

Available L1MU Triggers

- L1MU trigger terms
  - Loose == A
  - Tight == AC (CF), AB (EF)
- Implemented L1MU terms
  - MUO(count,PTX,eta,L,X,X)
  - MUO(count,PTX,eta,X,L,X)
  - MUO(count,PTX,eta,L,L,X)
  - MUO(count,PTX,eta,T,X,X)
  - MUO(count,PTX,eta,X,T,X)
  - MUO(count,PTX,eta,T,T,X)
  - MUO(2,PTX,eta,T,X,L)
- Additional terms can be implemented
  - Need feedback from physics groups
- L1MU.L1CFT terms deferred until fall

L1CFT Issue

- L1 Trigger Latency Problem
  - L1MU.L1CFT decision is ~250 ns longer than the ECB spec
  - We are not even at the ECB spec
- Solution 1
  - CFT clock goes from 132 to 264 ns
  - TF moves 2 big (132 ns) clock ticks back
  - TF does internal (60 ns) adjustment
  - All systems increase pipeline depth by 2 clock ticks
  - L1MU finds 132 ns in 05 logic

L1CFT Issue

- L1 Trigger Latency Problem
  - L1MU.L1CFT decision is ~250 ns longer than the ECB spec
  - We are not even at the ECB spec
- Solution 2
  - CFT clock goes from 132 to 264 ns
  - TF moves 3 big (132 ns) clock ticks back
  - TF does internal (60 ns) adjustment
  - TF sends L1 decision early on twist-n-flat to select PDT MFC cards
  - All systems increase pipeline depth by 3 clock ticks

L1MU Simulator

- Little change in last two months
- Previously showed <1% disagreement between hardware and simulator L1MU decisions using data
- In progress
  - RCP based algorithms
  - Updated RCP files to match FPGA algorithms (including dimuon)
  - L1MU to L2MU bug
  - L3 message re-ordering
  - online monitoring
  - updated documentation

mu1 Rates (preliminary)

TERM	RATE AT 2.5E20 (HZ)
MU1PTXCLXX	27600
MU1PTXCLLX	34200
MU1PTXCLLX	1500
MU1PTCTXX	231
MU1PTXCXTX	1928
MU1PTXCTTX	37

mu2 Rates (preliminary)

TERM	RATE AT 3.3E30 (HZ)
MU2PTXCLXX	540
MU2PTXCXLX	18900
MU2PTXCLLX	106
MU2PTXCTXL	24
MU2PTXCTXX	0.7
MU2PTXCXTX	391
MU2PTXCTTX	0.2

Conclusions

- Hardware commissioning rapidly winding down
- Algorithm commissioning rapidly heating up
- Many opportunities for physics groups to contribute by performing MC and data analysis studies, especially in the low Pt regime

Run II Muon Detector